

ABSTRACT OF THE DISCLOSURE

There is provided a semiconductor memory device in which a bit line precharge operation is increased in speed, and a layout area is reduced.

- 5 P-channel transistors (206, 207) that function as switches are provided in a precharge voltage pumping circuit (105) included in a bit line precharge voltage generation unit. This enhances a pumping efficiency, and reduces a capacitance area of a pumping capacitor (200).